

Highly-Integrated Green-Mode PWM Controller

SG6842

FEATURES

- Linearly-Decreasing PWM Frequency
- Burst-Mode
- Low Start-Up Current (8uA)
- Low Operating Current (3.7mA)
- Internal Latch Circuit (OTP, OVP)
- Leading-Edge Blanking
- Synchronized Slope Compensation
- Totem Pole Output with Soft Driving
- Improved EMI
- Constant Power Limit (Full AC Input Range)
- Current Mode Operation
- Cycle-by-Cycle Current Limiting
- Under Voltage Lockout (UVLO)
- Programmable PWM frequency
- GATE Output Maximum Voltage Clamp (18V)
- VDD Over Voltage Protection (OVP)
- Programmable Over Temperature Protection (OTP)
- Few External Components Required

APPLICATIONS

General-purpose switch mode power supplies and flyback power converters, including:

- Power Adapters
- Open-Frame SMPS
- Battery-Charger Adapters

DESCRIPTION

The highly integrated SG6842 series of PWM controllers provides several features to enhance the performance of flyback converters. To minimize standby power consumption, a proprietary green-mode function provides off-time modulation to linearly decrease the

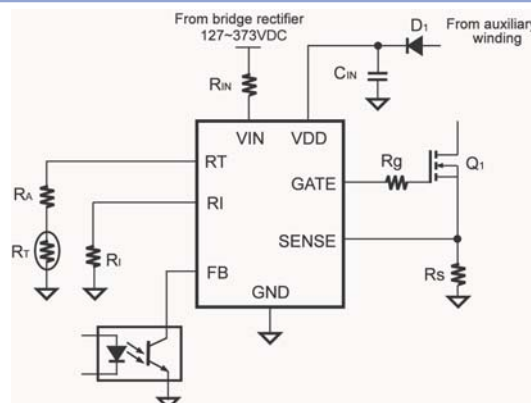
switching frequency under light-load conditions. Under zero-load conditions, the power supply enters burst-mode. This completely shuts off PWM output. Then, the output restarts just before the supply voltage, VDD, drops below the UVLO voltage. This green-mode function enables the power supply to easily meet international power conservation requirements.

For improved power conversion efficiency, the SG6842 series is manufactured using the BiCMOS process. This allows the start-up current to be reduced to 8uA, and the operating current to be reduced to 3.7mA. For even higher power conversion efficiency, a large start-up resistance can be used.

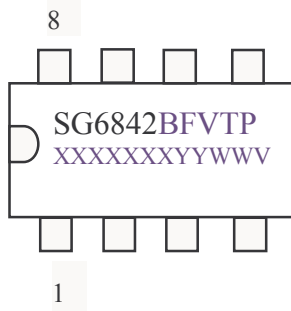
Built-in synchronized slope compensation ensures the stability of peak current mode control. Proprietary internal compensation ensures constant output power limiting over a universal range of AC input voltages, from 90VAC to 264VAC.

SG6842 controllers provide many protection functions. Pulse-by-pulse current limiting ensures a constant output current, even when short circuits occur. Should an open circuit failure occur in the feedback loop, the internal protection circuit will disable PWM output. PWM output will be disabled as long as VDD exceeds a threshold. The gate output is clamped at 18V to protect the power MOS from damage due to high voltage conditions. An external NTC thermistor can be applied to sense the ambient temperature for over temperature protection. When internal latch circuit is used to latch-off the controller, the latch will be reset when the power supply VDD is disabled.

SG6842 series controllers are available in both 8-pin DIP and SO packages.

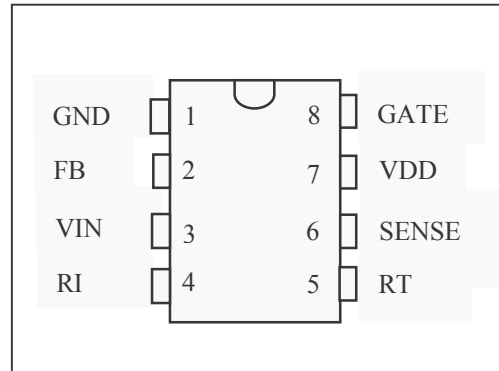
TYPICAL APPLICATION


MARKING DIAGRAMS



B: B = Linearly Decreasing Frequency + Burst-Mode
 F: L = OTP Latch: The pin is reset when AC is disconnected.
 C = Hysteresis OTP : The pin is reset when the temperature cools down.
 V: V = OVP Latch
 T: D = DIP, S = SOP
 P : Z =Lead Free + ROHS Compatible
 Null=regular package
 XXXXXXXX: Wafer Lot
 YY: Year; WW: Week
 V: Assembly Location

PIN CONFIGURATION



ORDERING INFORMATION

Part Number	Package
SG6842BLVS	8-Pin SOP
SG6842BLVD	8-Pin DIP
SG6842BLVSZ	8-Pin SOP(Lead Free)
SG6842BLVDZ	8-Pin DIP(Lead Free)
SG6842BCVS	8-Pin SOP
SG6842BCVD	8-Pin DIP
SG6842BCVSZ	8-Pin SOP(Lead Free)
SG6842BCVDZ	8-Pin DIP(Lead Free)

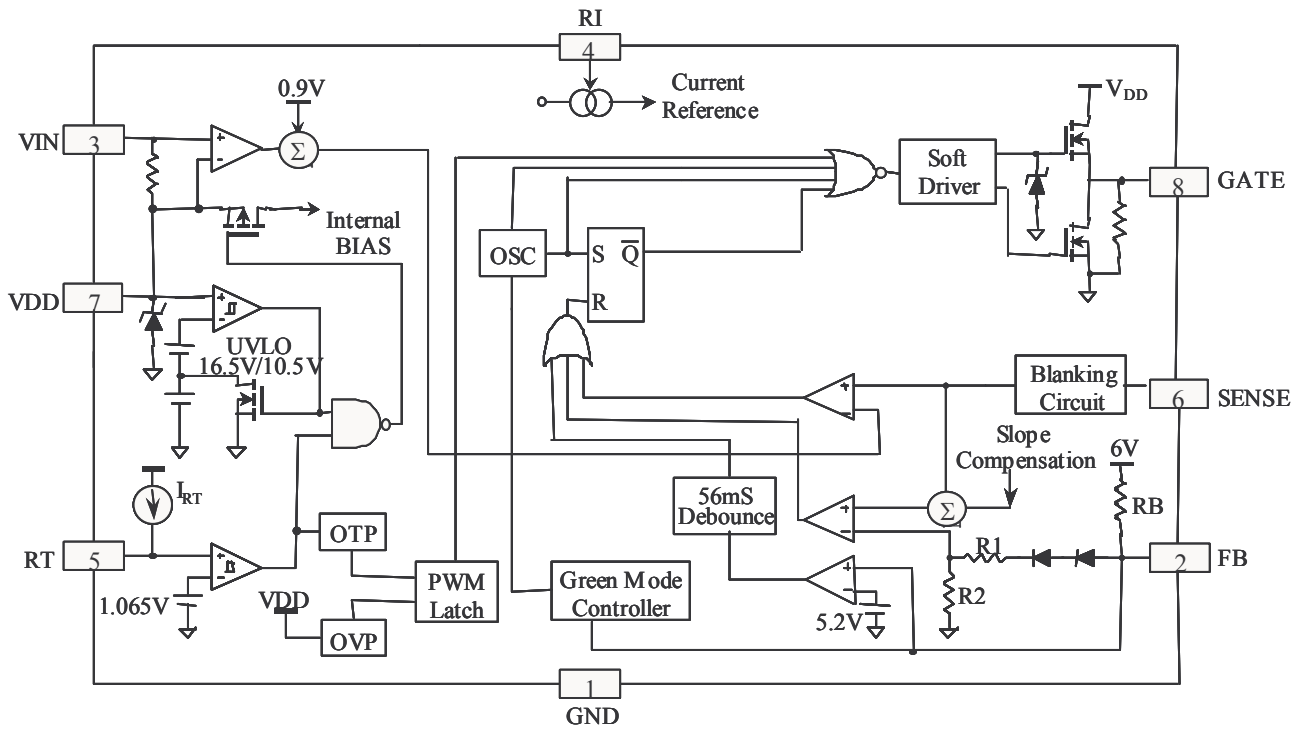
PIN DESCRIPTIONS

Pin No.	Symbol	Function	Description
1	GND	Ground	Ground.
2	FB	Feedback	The signal from the external compensation circuit is fed into this pin. The PWM duty cycle is determined in response to the signal from this pin and the current-sense signal from Pin 6.
3	VIN	Start-Up Input	For start-up, this pin is pulled high to the rectified line input. This pin is pulled via a resistor. Since the start-up current requirement of the SG6842 is very small, a large start-up resistance can be used to minimize power loss. Under normal operation, this pin is also used to detect the line voltage. The line voltage is detected to compensate the output power limit, so that it can be kept constant over a universal AC input range
4	RI	Reference Setting	A resistor connected from the RI pin to ground will provide the SG6842 with a constant current source. This current charges an internal capacitor. This determines the switching frequency. Increasing the resistance will decrease the amplitude of the current from the current source, and thereby reduce the switching frequency. Using a 26kΩ resistor R _I results in a 50uA constant current I _I and a 65kHz switching frequency.
5	RT	Temperature Detection	For over-temperature protection. An external NTC thermistor is connected from this pin to ground. The impedance of the NTC will decrease at high temperatures. Once the voltage of the RT pin drops below a fixed limit of 1.05V, PWM output will be disabled.

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6	SENSE	Current Sense	Current sense. The sensed voltage is used for current-mode control and pulse-by-pulse current limiting.
7	VDD	Power Supply	Power Supply. If an open circuit failure occurs in the feedback loop, the internal protection circuit will disable PWM output as long as VDD remains higher than 26V.
8	GATE	Driver Output	The totem-pole output driver for the power MOSFET. A soft driving waveform is implemented for improved EMI.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Condition	Value	Unit
V _{DD}	Supply Voltage	Low Impedance Source,	27	V
I _Z	Zener Current	-	10	mA
V _{IN}	Input Terminal		28	V
I _{SINK}	Error Amplifier Sink Current	-	10	mA
V _{FB}	Input Voltage to FB Pin	-	-0.3 to 7V	V
V _{Sense}	Input Voltage to SENSE Pin	-	-0.3 to 7V	V
V _{RT}	Input Voltage to RT Pin	-	-0.3 to 7V	V
V _{RI}	Input Voltage to RI Pin	-	-0.3 to 7V	V
P _D	Power Dissipation	at T _A < 50°C	DIP 800 SOP 400	mW
R _{θ ja}	Thermal Resistance	Junction-Air	DIP 82.5 SOP 141	°C/W
R _{θ jc}	Thermal Resistance	Junction-Case	DIP 67.1 SOP 41.2	°C/W
T _J	Operating Junction Temperature	-	150	°C
T _A	Operating Ambient Temperature	-	-40 to 125	°C
T _{STG}	Storage Temperature Range	-	-65 to +150	°C
T _L	Lead Temperature (Soldering)	10 sec	DIP 260 SOP 230	°C
	ESD Capability, HBM Model	-	2.0	kV

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V _{DD}	Supply Voltage	-	20	V
T _A	Operating Ambient Temperature	-30	85	°C

ELECTRICAL CHARACTERISTICS (V_{DD} =15V, TEMP =27°C)
V_{DD} Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V _{TH(ON)}	On Threshold Voltage		15.5	16.5	17.5	V
V _{TH(OFF)}	Off Threshold Voltage		9.5	10.5	11.5	V
I _{DD ST}	Start-Up Current	V _{DD} = 15V		8	30	µA
I _{DD OP}	Operating Supply Current	FB=SENSE=0V, V _{DD} =15V, GATE Open		3.7	5	mA
BLV _{VERSION} V _{DD-OVP}	V _{DD} Over Voltage Protection (Latch off).		24.5	25.5	26.5	V
BCV _{VERSION} V _{DD-OVP}	V _{DD} Over Voltage Protection (Latch off).		22.6	23.6	24.6	V
T _{D-VDD-OVP}	V _{DD} Over Voltage Protection Debounce (Disable PWM Output)	R _I =26kΩ		100		µsec
V _{DD-ZENER}	V _{DD} ZENER Crowbar	I _{DD} = 10mA	27	30	33	V
V _{DD-th-g}	V _{DD} Low-Threshold Voltage to Exit Green-OFF Mode		V _{TH(OFF)} + 0.8	V _{TH(OFF)} + 1.25	V _{TH(OFF)} + 1.7	V

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Feedback Input Section

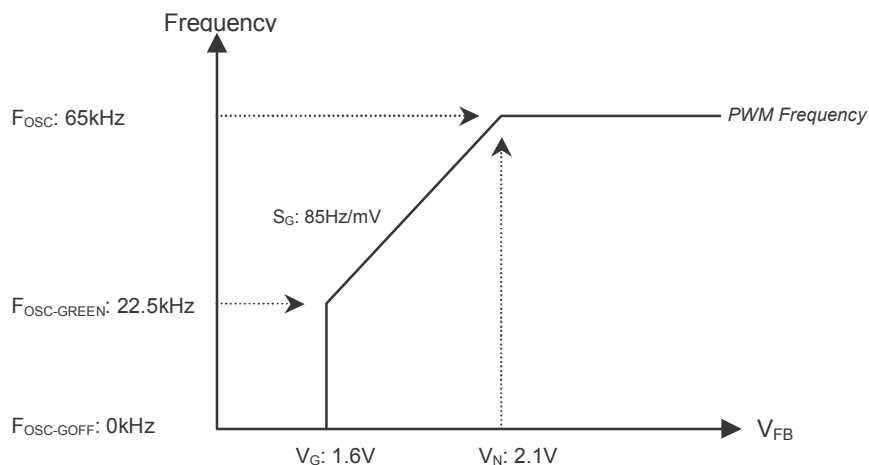
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
A_V	Input-Voltage to Current-Sense Attenuation		1/4.5	1/4	1/3.5	V/V
Z_{fb}	Input Impedance			4.5		k Ω
I_{fb}	Bias Current				2	mA
V_{FBP}	Protection Level for Limited Power Control			5.2		V
$T_{\text{delay-lps}}$	The Delay Time for Limited Power Control.	$V_{FB}=5.2V$ $R_I=26k\Omega$		56		msec
V_{FB0}	FB Pin open voltage			6.75		V

Current Sense Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Z_{cs}	Input Impedance			12		k Ω
T_{PD}	Delay to Output			100	200	nsec
$\Delta V_{TH @ I_{IN80UA}}$	Threshold Voltage Change versus VIN Pin Input Current	$I_{IN} = 80 \mu A, R_I=26K\Omega$	0.77	0.82	0.87	V
$\Delta V_{TH @ I_{IN160UA}}$	Threshold Voltage Change versus VIN Pin Input Current	$I_{IN} = 160 \mu A, R_I=26K\Omega$	0.72	0.77	0.82	V
B_{nk}	Leading Edge Blanking Time		260	360	460	nsec

Oscillator Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
F_{osc}	Normal Mode Frequency	$R_I=26K\Omega$	60	65	70	kHz
$F_{osc-green}$	Green-ON Mode Frequency	$R_I=26K\Omega$	20	22.5	25	kHz
V_G	Green-OFF Mode Voltage at FB pin	$V_{DD}=15V$	1.4	1.6	1.8	V
V_N	FB Pin Frequency Reduction Threshold	$V_{DD}=15V$	1.9	2.1	2.3	V
S_G	Green-Mode Modulation Slope	$R_I=26k\Omega$		85		Hz/mV
F_{dv}	Frequency Variation Versus V_{DD} Deviation	$V_{DD}=11.5$ to $20V$			5	%
F_{dt}	Frequency Variation Versus Temp. Deviation	$T_A=-30$ to $85^\circ C$		1.5	5	%



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PWM Output Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DCY (MAX)	Maximum Duty Cycle		80	85	90	%
V _{ol}	Output Voltage Low	V _{DD} = 12V, I _O = 50mA			1.5	V
V _{oh}	Output Voltage High	V _{DD} = 12V, I _O = 50mA	8V			V
T _R	Rising Time	V _{DD} = 15V, C _L = 1nF	150	250	350	nsec
T _F	Falling Time	V _{DD} = 15V, C _L = 1nF	30	50	90	nsec
V _{clamp}	Gate Output Clamping Voltage	V _{DD} = 25V		18		V

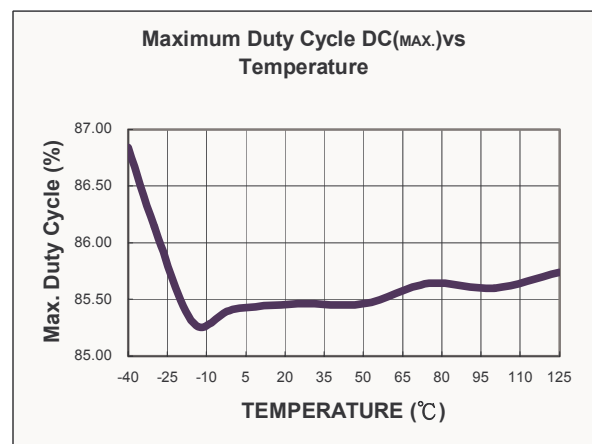
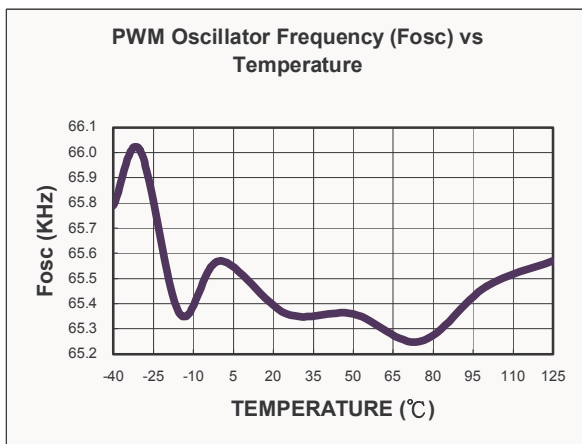
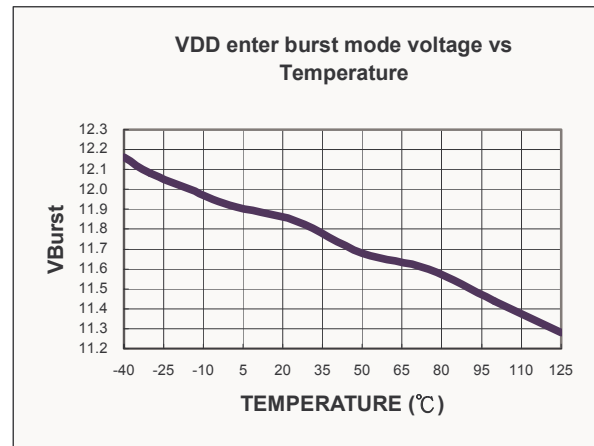
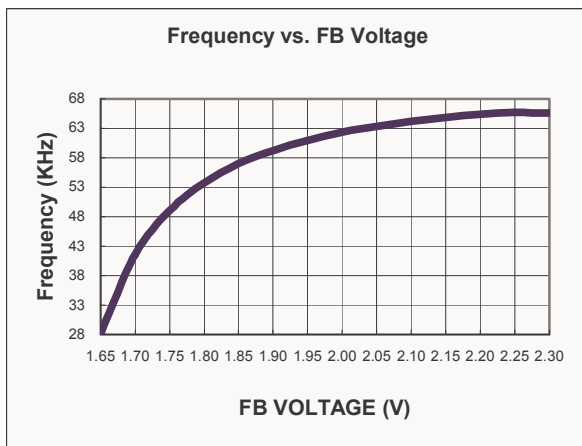
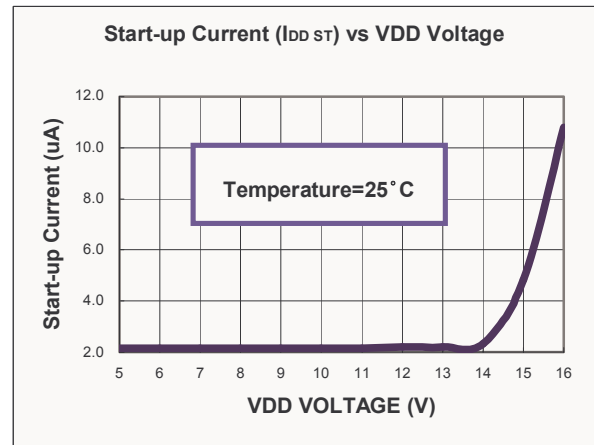
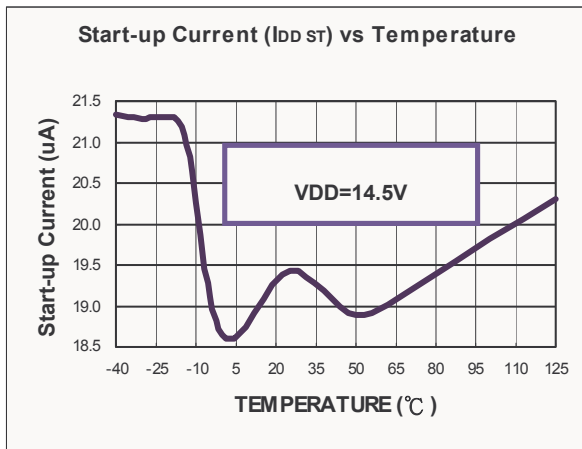
Over Temperature Protection Section

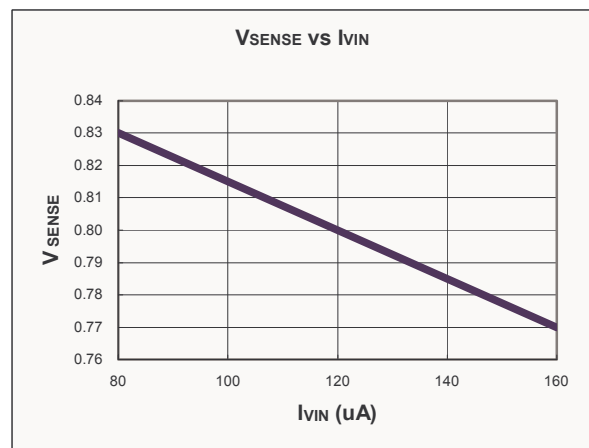
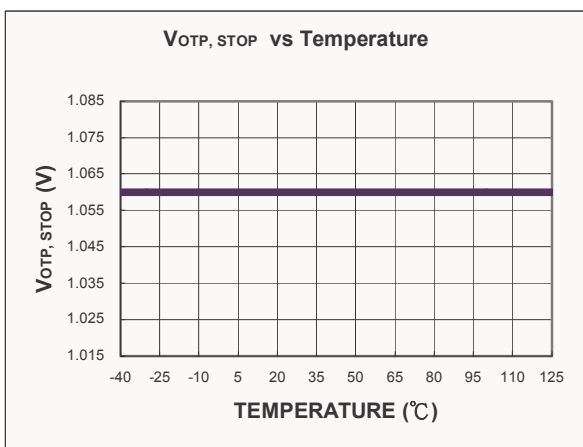
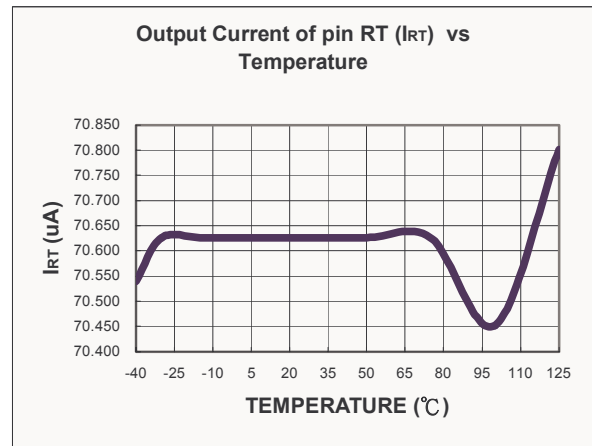
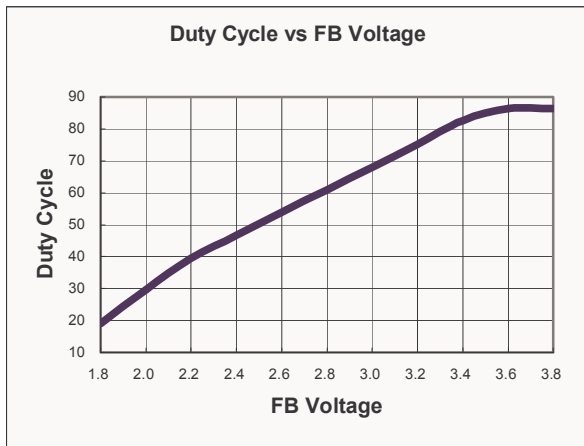
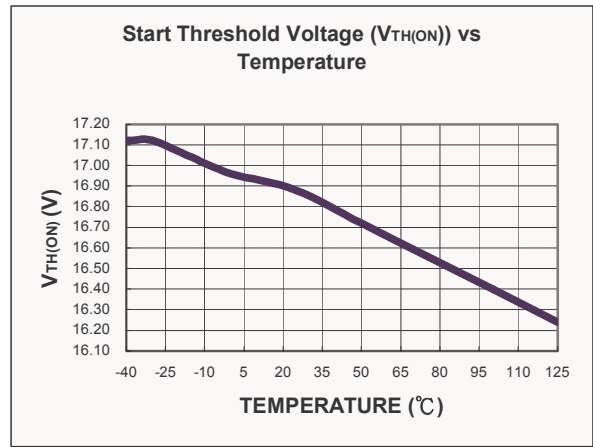
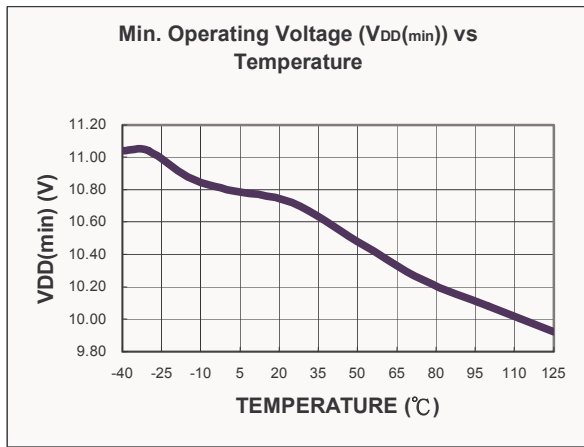
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I _{rt}	Output Current of RT Pin	R _t = 26kΩ	64	70	76	μA
V _{OTP-OFF}	OTP turn-off level		1.015	1.065	1.115	V
BCV _{VERSION}	OTP release level		V _{OTP-OFF}	V _{OTP-OFF}	V _{OTP-OFF}	V
V _{OTP-RESET-ON}			+0.06	+0.1	+0.14	
T _{DOTP-LATCH}	Over-Temperature Latch-Off Debounce	R _t = 26kΩ	60	100	140	μsec

RI Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R _{I-NOR}	R _i Operating Range		15.5		36	kΩ
R _{I-MAX}	Max. R _i value for Protection			216		kΩ
R _{I-MIN}	Min. R _i value for Protection			6		kΩ

TYPICAL CHARACTERISTICS





OPERATION DESCRIPTION

Start-Up Current

The typical start-up current is only 8uA. This allows a high resistance, low-wattage start-up resistor to be used, to minimize power loss. A 1.5 MΩ, 0.25W, start-up resistor and a 10uF/25V VDD hold-up capacitor would be sufficient for an AC/DC adapter with a universal input range.

Operating Current

The required operating current has been reduced to 3.7mA. This results in higher efficiency and reduces the VDD hold-up capacitance requirement.

Green-Mode Operation

The proprietary Green-mode function provides off-time modulation to linearly decrease the switching frequency under light-load conditions. On-time is limited to provide protection against abnormal conditions and brownouts. To further reduce power consumption under zero-load conditions, PWM output will be completely turned off, and the power supply will enter burst-mode. After the PWM oscillator is turned off, the IC's supply voltage VDD will drop gradually. Before the VDD voltage drops below the UVLO voltage, the PWM oscillator will be turned on again. This Green-mode function dramatically reduces power consumption under light-load and zero-load conditions. Power supplies using a SG6842 controller can easily meet even the most restrictive international regulations regarding standby power consumption.

Oscillator Operation

A resistor connected from the RI pin to ground generates a constant current source for the SG6842 controller. This current is used to charge an internal capacitor. The charge of the capacitor determines the internal clock period and the switching frequency. Increasing the resistance will decrease the amplitude of the current source and reduce the switching frequency. Using a 26kΩ resistor R_I results in a 50uA constant current I_I, and a corresponding 65kHz switching

frequency. The relationship between R_I and the switching frequency is:

$$f_{\text{PWM}} = \frac{1690}{R_I \text{ (k}\Omega\text{)}} \text{ (kHz)} \text{ ----- (1)}$$

Leading Edge Blanking

Each time the power MOSFET is switched on, a turn-on spike will inevitably occur at the sense-resistor. To avoid premature termination of the switching pulse, a 360nsec leading-edge blanking time is built in. Conventional RC filtering is not necessary. During this blanking period, the current-limit comparator is disabled, and it cannot switch off the gate drive.

Under-Voltage Lockout (UVLO)

The turn-on/turn-off thresholds are fixed internally at 16.5V/10.5V. To enable a SG6842 controller during start-up, the hold-up capacitor must first be charged to 16.5V through the start-up resistor.

The hold-up capacitor will continue to supply VDD before energy can be delivered from the auxiliary winding of the main transformer. VDD must not drop below 10.5V during this start-up process. This UVLO hysteresis window ensures that the hold-up capacitor can adequately supply VDD during start-up.

Gate Output / Soft Driving

The SG6842 BiCMOS output stage is a fast totem pole gate driver. Cross-conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 18V Zener diode in order to protect the power MOSFET transistors from any harmful over-voltage gate signals. A soft driving waveform is implemented to minimize EMI.

Slope Compensation

The sensed voltage across the current sense resistor is used for current-mode control and pulse-by-pulse current limiting. The built-in slope compensation function improves power supply stability and prevents peak current-mode control from causing sub-harmonic

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oscillations. With every switching cycle, the SG6842 controller produces a positively-sloped, synchronized ramp signal.

Constant Output Power Limit

When the SENSE voltage across the sense resistor R_S reaches the threshold voltage (around 0.85V), the output GATE drive will be turned off following a small propagation delay t_D . This propagation delay will result in an additional current proportional to $t_D \cdot V_{IN}/L_P$. The propagation delay is nearly constant regardless of the input line voltage V_{IN} . Higher input line voltages will result in larger additional currents. Thus, under high input-line voltages the output power limit will be higher than under low input-line voltages.

The output power limit variation can be significant over a wide range of AC input voltages. To compensate for this, the threshold voltage is adjusted by the current I_{IN} . Since the pin VIN is connected to the rectified input line voltage through the start-up resistor, a higher line voltage will result in a higher current I_{IN} through the pin VIN.

The threshold voltage decreases if the current I_{IN} increases. A small threshold voltage will force the output GATE drive to terminate earlier, thus reducing total PWM turn-on time, and making the output power equal to that of the low line input. This proprietary internal compensation feature ensures a constant output power limit over a wide range of AC input voltages (90VAC to 264VAC).

VDD Over-Voltage Protection

VDD over-voltage protection has been built in to prevent damage due to over voltage conditions. When the voltage VDD exceeds 25.5V due to abnormal conditions, PWM output will be turned off. Over-voltage conditions are usually caused by open feedback loops.

Thermal Protection

An external NTC thermistor can be connected from the RT pin to ground. The impedance of the NTC will

decrease at high temperatures. When the voltage of the RT pin drops below 1.065V, PWM output will be disabled.

Limited Power Control

The FB voltage will increase every time the output of the power supply is shorted or over-loaded. If the FB voltage remains higher than a built-in threshold (5.2V) for longer than 56msec, PWM output will then be turned off. As PWM output is turned off, the supply voltage VDD will also begin decreasing.

When VDD goes below the turn-off threshold (eg, 10.5V) the controller will be totally shut down. VDD will be charged up to the turn-on threshold voltage of 16.5V through the start-up resistor until PWM output is restarted. This protection feature will continue to be activated as long as the over-loading condition persists. This will prevent the power supply from overheating due to over loading conditions.

Protection Latch Circuit

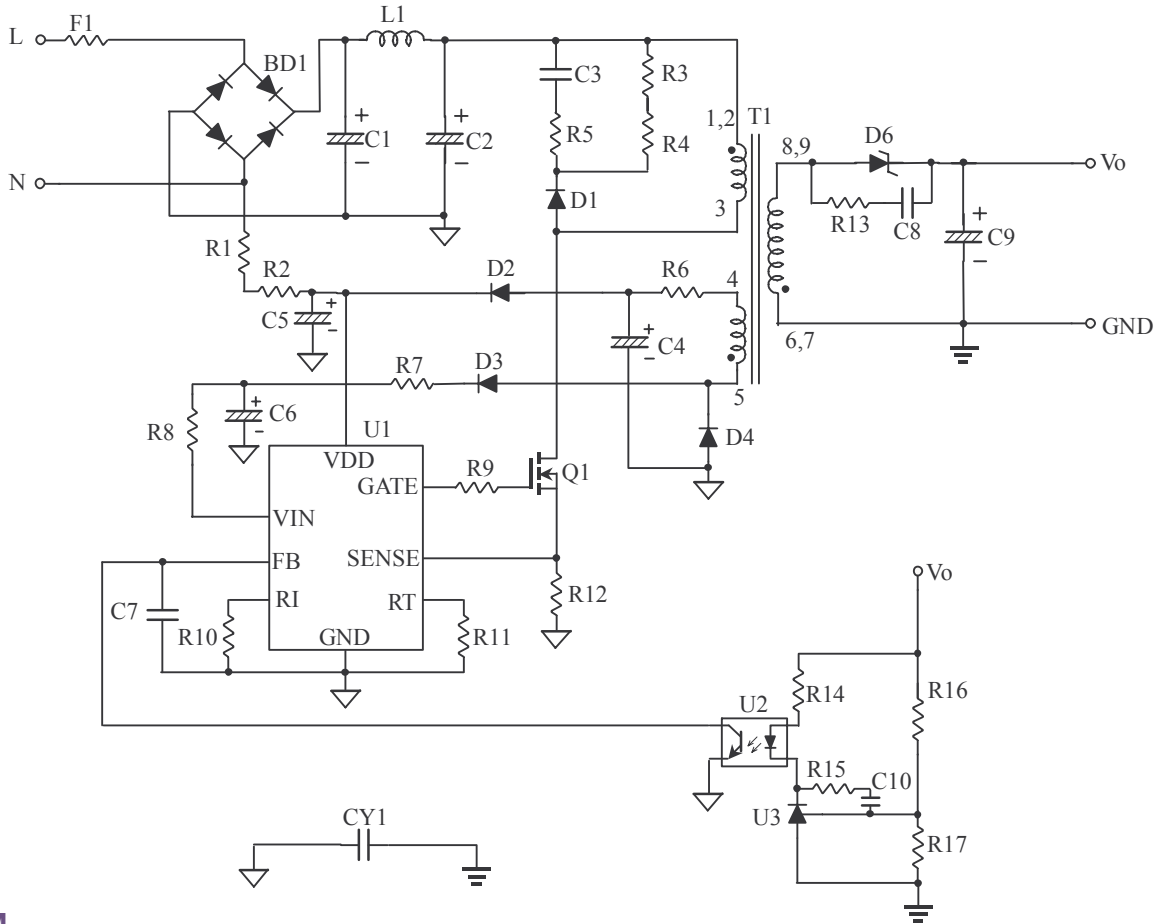
For the SG6842 family, the built-in latch function provides a versatile protection feature that does not require external components. See ordering information for a detailed description. To reset the latch circuit, it is necessary to remove the supply voltage from VDD pin

Noise Immunity

Noise from the current sense or the control signal may cause significant pulse width jitter, particularly in continuous-conduction mode. Slope compensation helps alleviate this problem. Good placement and layout practices should be followed. The designer should avoid long PCB traces and component leads. Compensation and filter components should be located near the SG6842. Finally, increasing the power-MOS gate resistance is advised.

REFERENCE CIRCUIT

Circuit (12V/5A)

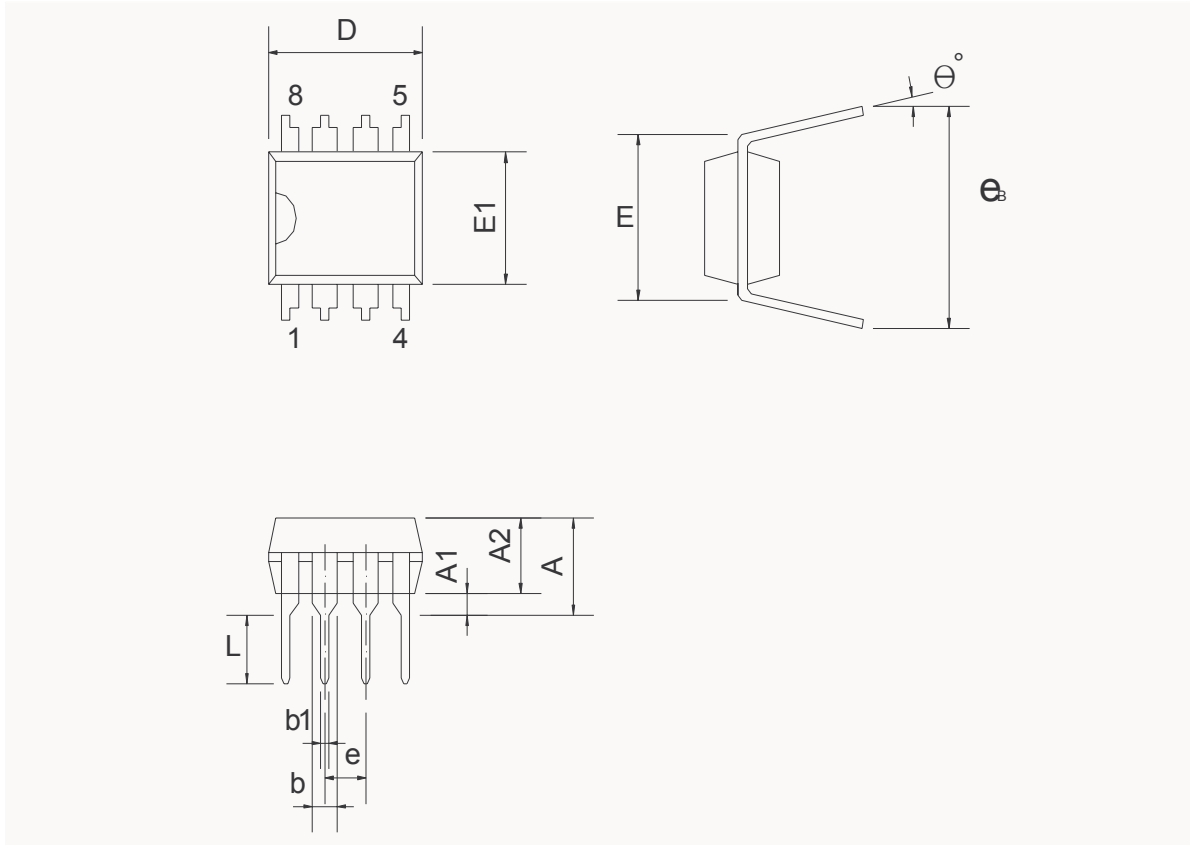


BOM

Reference	Component	Reference	Component
F1	FUSE 4A/250V	C9	EC 1000uF/25V
BD1	BD 4A/600V	R1,R2	R 330kΩ 1/4W
CY1	YC 222P/250V	R3,R4	R 47kΩ 1/4W
L1	UU10.5-10mH	R5	R 47Ω 1/4W
U1	IC SG6842	R6	R 10Ω 1/4W
U2	IC PC-817	R7	R 1KΩ 1/4W
U3	IC TL431	R8	R 470kΩ 1/8W
T1	Transformer PQ2620	R9,R13	R 51Ω 1/4W
D1	BYV95C	R10	R 26kΩ 1/8W 1%
D2,D3,D4	FR103	R11	Thermistor NTC 10K
C1,C2	EC 56uF/400V	R12	R 0.34Ω 1W 1%
C3	CC 103P/500V	R14	R 220Ω 1/4W
C4	EC 10uF/50V	R15	R 4.7kΩ 1/8W
C5	EC 4.7uF/50V	R16	R 154kΩ 1/8W 1%
C6,C8	CC 102P/200V	R17	R 39kΩ 1/8W 1%
C7,C10	CC 222P/50V	Q1	MOS PHX7NQ60E

PACKAGE INFORMATION

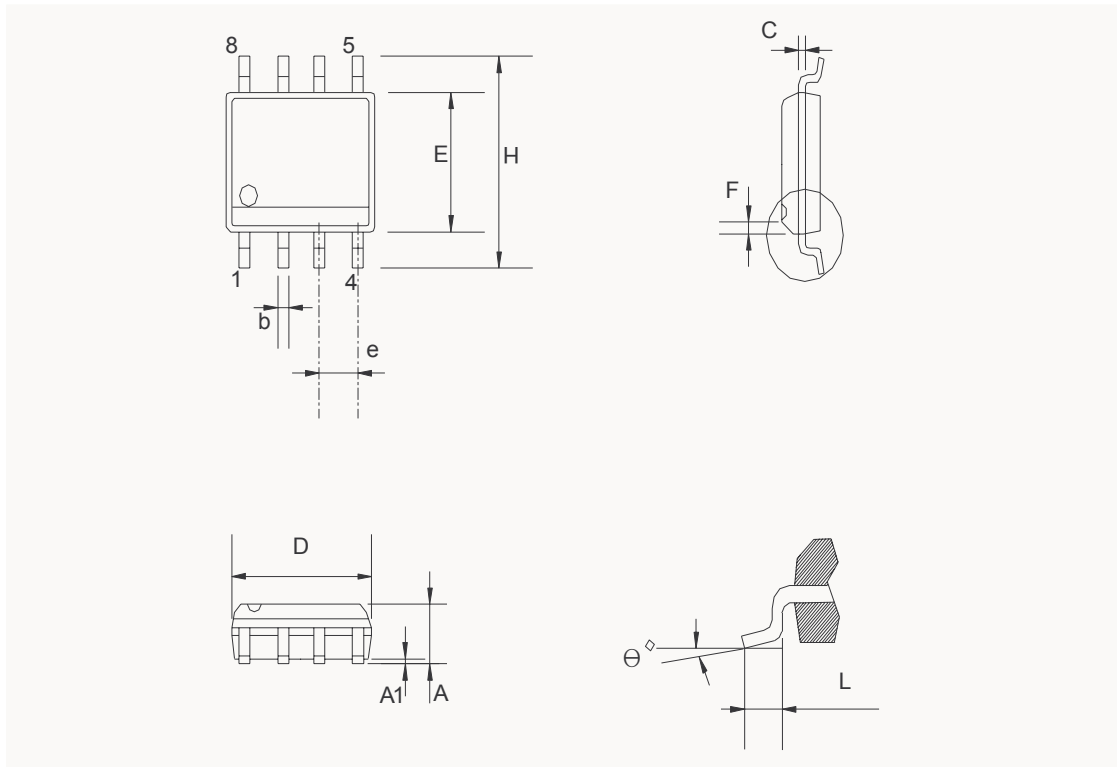
DIP-8 Outline Dimensions



Dimensions

Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.334			0.210
A1	0.381			0.015		
A2	3.175	3.302	3.429	0.125	0.130	0.135
b		1.524			0.060	
b1		0.457			0.018	
D	9.017	9.271	10.160	0.355	0.365	0.400
E		7.620			0.300	
E1	6.223	6.350	6.477	0.245	0.250	0.255
e		2.540			0.100	
L	2.921	3.302	3.810	0.115	0.130	0.150
eB	8.509	9.017	9.525	0.335	0.355	0.375
theta°	0°	7°	15°	0°	7°	15°

SOP-8 Outline Dimensions



Dimensions

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.346		1.752	0.053		0.069
A1	0.101		0.254	0.004		0.010
b		0.406			0.016	
c		0.203			0.008	
D	4.648		4.978	0.183		0.196
E	3.810		3.987	0.150		0.157
e	1.016	1.270	1.524	0.040	0.050	0.060
F		0.381X45°			0.015X45°	
H	5.791		6.197	0.228		0.244
L	0.406		1.270	0.016		0.050
θ°	0°		8°	0°		8°

DISCLAIMERS

LIFE SUPPORT

System General's products are not designed to be used as components in devices intended to support or sustain human life. Use of System General's products in components intended for surgical implant into the body, or other applications in which failure of System General's products could create a situation where personal death or injury may occur, is not authorized without the express written approval of System General's Chief Executive Officer. System General will not be held liable for any damages or claims resulting from the use of its products in medical applications.

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